layer, and the fifth layer as the side wall, and the boundary trench being disposed between the gate trench and the diode region and having a boundary side wall that faces the diode region

The gate insulating film covers the side walls of the trenches. The trench electrode is provided in the trenches via the gate insulating film. The interlayer insulating film is provided on the first surface of the semiconductor substrate and has an IGBT opening and a diode opening, the IGBT opening exposing the first layer and the second layer, and the diode opening exposing part of the fourth layer. The first electrode is provided on the interlayer insulating film, is in contact with the first layer and the second layer through the IGBT opening, and is in contact with the fourth layer through the diode opening. The second electrode is provided on the second surface of the semiconductor substrate and is in contact with the sixth layer and the seventh layer,

The fourth layer includes a trench-covering well region that covers a deepest part of the boundary side wall, a plurality of isolated well regions that are disposed separately from the trench-covering well region, and a diffusion region that connects the trench-covering well region and the plurality of isolated well regions. The diffusion region has a lower impurity concentration than impurity concentrations of the trench-covering well region and the isolated well regions when impurity concentrations in a direction parallel to the first surface of the semiconductor substrate are compared. The first electrode is in contact with the isolated well regions and away from the diffusion region.

A power semiconductor device according to another aspect of the present invention has a trench gate type IGBT region and a diode region for reverse conduction of the IGBT region. The power semiconductor device includes a semiconductor substrate, a gate insulating film, a trench electrode, an interlayer insulating film, a first electrode, and a second electrode.

The semiconductor substrate has a first surface and a second surface opposite the first surface, the first surface having a portion included in the IGBT region and a portion included in the diode region. The semiconductor substrate includes a first layer of a first conductivity type, a second layer of a second conductivity type different from the first conductivity type, a third layer of the second conductivity type, a fourth layer of the second conductivity type, a fifth layer of the first conductivity type, a sixth layer of the second conductivity type, and a seventh layer of the first conductivity type. The first layer is provided on the first surface and away from the second surface in the IGBT region. The second layer is provided on the first surface and away from the second surface in the IGBT region. The third layer is provided away from the first surface and the second surface in the IGBT region and is in contact with the first layer and the second layer. The fourth layer has a portion included in the diode region and is provided on the first surface and away from the second surface. The fifth layer is in contact with the third layer in the IGBT region and is in contact with the fourth layer in the diode region. The sixth layer is provided on the second surface, is at least partially included in the IGBT region, and is in contact with the fifth layer. The seventh layer is provided on the second surface, is at least partially included in the diode region, and is in contact with the fifth layer. The first surface of the semiconductor substrate is provided with a plurality of trenches each having a side wall. The plurality of trenches includes a gate trench and a boundary trench, the gate trench having a gate side wall that has a surface formed of the first layer, the third layer, and the fifth layer as the side wall, and the boundary trench being disposed between the gate trench and the diode region and having a boundary side wall that faces the diode region.

The gate insulating film covers the side walls of the trenches. The trench electrode is provided in the trenches via the gate insulating film. The interlayer insulating film is provided on the first surface of the semiconductor substrate and has an IGBT opening and a diode opening, the IGBT opening exposing the first layer and the second layer, and the diode opening exposing part of the fourth layer. The first electrode is provided on the interlayer insulating film, is in contact with the first layer and the second layer through the IGBT opening, and is in contact with the fourth layer through the diode opening. The second electrode is provided on the second surface of the semiconductor substrate and is in contact with the sixth layer and the seventh layer.

The fourth layer includes a trench-covering well region that covers a deepest part of the boundary side wall, a plurality of isolated well regions that are disposed separately from the trench-covering well region, a diffusion region that connects the trench-covering well region and the plurality of isolated well regions, and a high-concentration region. When impurity concentrations in a direction parallel to the first surface of the semiconductor substrate are compared, the diffusion region has a lower impurity concentration than impurity concentrations of the trench-covering well region and the isolated well regions, and the high-concentration region has a higher impurity concentration than impurity concentrations of the trench-covering well region and the isolated well regions. The first electrode is in contact with only the high-concentration region of the fourth layer.

A power semiconductor device according to yet another aspect of the present invention has an IGBT region that includes a plurality of cells, and a diode region for reverse conduction of the IGBT region. The power semiconductor device includes a semiconductor substrate, an interlayer insulating film, a first electrode, and a second electrode.

The semiconductor substrate has a first surface and a second surface opposite the first surface, the first surface having a portion included in the IGBT region and a portion included in the diode region. The semiconductor substrate includes a first layer of a first conductivity type, a second layer of the first conductivity type, and a third layer of a second conductivity type different from the first conductivity type. The first layer is provided on the second surface and is at least partially included in the diode region. The second layer is in contact with the first layer in the diode region. The third layer is provided on the first surface and away from the second surface, is at least partially included in the diode region, and is in contact with the second layer.

The interlayer insulating film is provided on the first surface of the semiconductor substrate and has a diode opening that exposes part of the third layer. The first electrode is provided on the interlayer insulating film and is in contact with the third layer through the diode opening. The second electrode is provided on the second surface of the semiconductor substrate and is in contact with the first layer.

The third layer includes a first region and a plurality of second regions, the first region being provided on the whole of the first surface in the diode region, the plurality of second regions being spaced from each other on the first region. When impurity concentrations in a direction parallel to the first surface of the semiconductor substrate are compared, the second region has a higher impurity concentration than